ABSTRACT

A semiconductor memory device having a plurality of memory blocks, each block including a plurality of memory banks is disclosed, which can be accurately operated with high speed, and which consumes less power. The device comprises a row decoding section for decoding the row address so as to generate a row selecting signal; and a column decoding section, adjacent to the row decoding section, for decoding the column address so as to generate a column selecting signal. The word lines driven by the row selecting signal and column selecting signal lines for outputting the column selecting signal are arranged parallel to each other, so as to supply these signals to the memory block of a target memory cell and to access the memory cell.